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Results 1 - 10 of about 1,010 for digital/analog simulation. (0.15 seconds)

Digital analog simulation of uniform motion in representations of physical n-space by lattice-work ... - group of 2 »

AM Shende - 1991 - adsabs.harvard.edu

Title: **Digital Analog Simulation** of Uniform Motion in Representations of Physical N-Space by Lattice-Work Mimd Computer Architectures Authors: Shende, Anil ...

Cited by 8 - [Web Search](#) - [Library Search](#)

VHDL-AMS-a hardware description language for analog and mixed-signal applications - group of 3 »

E Christen, K Bakalar - IEEE Transactions on Circuits and Systems II: Analog and ..., 1999 - ieeexplore.ieee.org

... Analog **simulation**, hardware description lan- guages, mixed-signal **simulation**, VHDL-AMS. ... HDL's can be divided into **digital**, **analog**, and mixed- signal HDL's ...

Cited by 80 - [Web Search](#) - [BL Direct](#)

A Module Generator for High-Speed CMOS Current Output Digital/Analog Converters - group of 4 »

RR Neff, PR Gray, A Sangiovanni-Vincentelli - IEEE Journal of Solid-State Circuits, 1996 - ieeexplore.ieee.org

... California, Berkeley Abstract This paper presents a module generator for **Digital/Analog** Converter (DAC) circuits. A combination of circuit **simulation** and ...

Cited by 13 - [Web Search](#) - [BL Direct](#)

A mathematical model for the continuous culture of microorganisms utilizing inhibitory substrates - group of 2 »

JF Andrews - Biotechnology and Bioengineering, 1968 - doi.wiley.com

... However, these equations can be solved using the analog computer or one of the **digital-analog simulation** prgrams.. The solutions presented in this paper were ...

Cited by 123 - [Web Search](#)

Fault simulation of linear analog circuits - group of 4 »

N Nagi, A Chatterjee, JA Abraham - Journal of Electronic Testing, 1993 - Springer

... Fault **Simulation** of Linear Analog Circuits ... An efficient fault **simulation** is then performed on this discretized circuit for the given input test wave form. ...

Cited by 27 - [Web Search](#) - [BL Direct](#)

[BOOK] A guide to simulation - group of 2 »

P Bratley, BL Fox, LE Schrage - 1987 - books.google.com

A Guide to **Simulation** Springer New York Berlin Heidelberg Barcelona Budapest HongKong London Milan Paris Santa Clara Singapore Tokyo ... A Guide to **Simulation** ...

Cited by 720 - [Web Search](#) - [Library Search](#)

[CITATION] A survey of digital simulation—Digital analog simulator programs.

RD Brennan, RN Linebarger - **Simulation**, 1964

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Evolution of Continuous-Time Modeling and Simulation - group of 7 »

KJ Astroem, H Elmqvist, SE Mattson - ESM, 1998 - diquima.upm.es

The 12th European **Simulation** Multiconference, ESM'98, June 16--19, 1998, Manchester, UK EVOLUTION OF CONTINUOUS-TIME MODELING AND **SIMULATION** ... ANALOG **SIMULATION** ...

Cited by 28 - [View as HTML](#) - [Web Search](#)

A DYNAMIC MODEL OF THE ANAEROBIC DIGESTION PROCESS

JF ANDREWS - 1969 - csa.com

... **SIMULATION** STUDIES, UTILIZING A **DIGITAL-ANALOG SIMULATION** PROGRAM (PACTOLUS), OF BOTH BATCH AND CONTINUOUS FLOW SYSTEMS PROVIDED ADDITIONAL EVIDENCE BY ...

Cited by 18 - [Web Search](#)

[BOOK] CMOS analog circuit design

PE Allen, DR Holberg - 1996 - books.google.com
... 6.5 Cascode Op Amps 293 6.6 **Simulation** and Measurement of Op Amps 3 10 ... References
61 1 Chapter 10 **Digital—Analog** and Analog—Digital Converters 612 ...
Cited by 469 - Web Search - Library Search

PE Allen, DR Holberg - 1996 - books.google.com
... 6.5 Cascode Op Amps 293 6.6 **Simulation** and Measurement of Op Amps 3 10 ... References
61 1 Chapter 10 **Digital—Analog** and Analog—Digital Converters 612 ...
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PE Allen, DR Holberg - 1996 - books.google.com
... 6.5 Cascode Op Amps 293 6.6 **Simulation** and Measurement of Op Amps 3 10 ... References
61 1 Chapter 10 **Digital—Analog** and Analog—Digital Converters 612 ...
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PE Allen, DR Holberg - 1996 - books.google.com
... 6.5 Cascode Op Amps 293 6.6 **Simulation** and Measurement of Op Amps 3 10 ... References
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Physical and scalable IV model in BSIM 3 v 3 for **analog/digital** circuit **simulation** - group of 4 »

Y Cheng, MC Jeng, Z Liu, J Huang, M Chan, K Chen, ... - IEEE Transactions on Electron Devices, 1997 - [ieeexplore.ieee.org](#)

... BSIM3v3 for **Analog/Digital** Circuit **Simulation** Yuhua Cheng, Member, IEEE, Min-Chie

Jeng, Member, IEEE, Zhihong Liu, Member, IEEE, Jianhui Huang, ...

Cited by 53 - [Web Search](#) - [BL Direct](#)

Simulation of mixed switched-capacitor/digital networks with signal-driven switches - group of 4 »

K Suyama, SC Fang, YP Tsvividis - IEEE Journal of Solid-State Circuits, 1990 - [ieeexplore.ieee.org](#)

... **Simulation** re- suits for a PCM voice encoder, a sigma—delta modulator, a ... I. INTRODUCTION

A N IMPORTANT class of mixed **analog—digital** VLSI circuits can be ...

Cited by 19 - [Web Search](#)

FOCUS: An Experimental Environment for Fault Sensitivity Analysis - group of 4 »

GS Choi, RK Iyer - IEEE Transactions on Computers, 1992 - [portal.acm.org](#)

... Carreno, G. Choi, and R. Iyer, "**Analog-digital simulation** of transient-induced logic

errors and upset susceptibility of an advanced control system," NASA Tech. ...

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All-Optical Gain Control of In-Line Erbium-Doped Fiber Amplifiers for Hybrid **Analog/Digital** WDM ... - group of 2 »

H Dai, JY Pan, C Lin - IEEE PHOTONICS TECHNOLOGY LETTERS, 1997 - [ieeexplore.ieee.org](#)

... erbium-doped fiber amplifiers (EDFA's) used in hybrid **analog/digital** wavelength

division ... EDFA ASE peak of 1532 nm), our **simulation** shows that lasing action ...

Cited by 17 - [Web Search](#) - [BL Direct](#)

An integrated **analog/digital** random noise source - group of 4 »

WT Holman, JA Connelly, AB Dowlatabadi - IEEE Transactions on Circuits and Systems I Fundamental ..., 1997 -

[ieeexplore.ieee.org](#)

... the integrated noise source (INS), a high performance **analog/digital** random noise ...

pseudorandom numeric sequences for the purposes of **simulation** or circuit test ...

Cited by 22 - [Web Search](#) - [BL Direct](#)

Simulating Mixed **Analog-Digital** Circuits on a Digital Simulator - group of 2 »

D Thelen, J MacDonald - Proc. ICCAD-88, 1988 - [ieeexplore.ieee.org](#)

... A technique for modeling such analog circuits as "digital" behavior models has been

developed and **simulation** of mixed **analog-digital** circuits based on this ...

Cited by 4 - [Web Search](#)

[BOOK] CMOS analog circuit design

PE Allen, DR Holberg - 1996 - [books.google.com](#)

... the role of subsystem components, partitioned at **analog—digital** boundaries, they ...

modeling of electronic components, computer **simulation** techniques, Laplace ...

Cited by 469 - [Web Search](#) - [Library Search](#)

A Digital Background Calibration Technique for Time-Interleaved Analog-to-Digital Converters - group of 4 »

D Fu, KC Dyer, SH Lewis, PJ Hurst - IEEE Journal of Solid-State Circuits, 1998 - [ieeexplore.ieee.org](#)

... Index Terms—Adaptive systems, **analog—digital** conversion, cal- ibration, CMOS analog

integrated ... According to **simulation**, in the first three stages of each ...

Cited by 44 - [Web Search](#) - [BL Direct](#)

Simulation techniques for mixed **analog/digital** circuits - group of 3 »

EL Acuna, JP Dervenis, AJ Pagones, FL Yang, RA ... - IEEE Journal of Solid-State Circuits, 1990 - [ieeexplore.ieee.org](#)

... Page 3. ACUNA et d.: **SIMULATION** TECHNIQUES FOR MIXED **ANALOG/DIGITAL** CIRCUITS 355 ...

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Title: Mixed **analog/digital** VLSI design and **simulation** of an adaptive resonance theory (ART) neural network architecture **Authors:** Liou, Juin J.; Ho, Ching S ...

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Results 1 - 10 of about 28,400 for mixed signal simulation. (0.16 seconds)

[BOOK] **Simulation techniques and solutions for mixed-signal coupling in integrated circuits**

NK Verghese, TJ Schmerbeck, DJ Allstot - 1995 - books.google.com

... **SIMULATION TECHNIQUES AND SOLUTIONS FOR MIXED-SIGNAL COUPUNG IN IC.** 4.1 Simplified Equation ... **SIMULATION TECHNIQUES AND SOLUTIONS FOR MIXED-SIGNAL COUPUNG IN IC.** ...

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Creating a Mixed-Signal Simulation Capability for Concurrent IC Design and Test Program Development - group of 4 »

T Austin - PROC INT TEST CONF., IEEE, IEEE SERVICE CENTER, PISCATAWAY, ..., 1993 - [ieeexplore.ieee.org](#)

Page 1 0-7803-1429-8/93 \$3.00 © 1993 IEEE 125 Creating a **Mixed-Signal Simulation**

Capability for Concurrent IC Design and Test Program Development Tom Austin ...

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VHDL-AMS-a hardware description language for analog and mixed-signal applications - group of 3 »

E Christen, K Bakalar - ... on Circuits and Systems II: Analog and Digital **Signal** ..., 1999 - [ieeexplore.ieee.org](#)

... illustrating them by examples. Index Terms— Analog **simulation**, hardware description lan- guages, **mixed-signal simulation**, VHDL-AMS. ...

Cited by 80 - [Web Search](#) - [BL Direct](#)

Efficient Techniques for Accurate Modeling and Simulation of Substrate Coupling in Mixed-Signal IC's - group of 12 »

JP Costa, M Chou, LM Silveira - IEEE TRANSACTIONS ON COMPUTER AIDED DESIGN OF INTEGRATED ..., 1999 - [ieeexplore.ieee.org](#)

... the analog Page 3. COSTA et al.: ACCURATE MODELING AND **SIMULATION OF SUBSTRATE COUPLING IN MIXED-SIGNAL IC'S** 599 Fig. 3. Cross ...

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Simulation of substrate coupling in mixed-signal MOS circuits - group of 2 »

S Masui - Proceedings of the IEEE International Symposium on VLSI ..., 1992 - [ieeexplore.ieee.org](#)

Page 1 **Simulation** of Substrate Coupling in **Mixed-Signal** MOS Circuits Shoichi Masui*

Electsical Engineering Department, Stanford University Stanford, CA 94305 5 ...

Cited by 33 - [Web Search](#)

Synthesis Tools for Mixed-Signal ICs: Progress on Frontend and Backend Strategies - group of 9 »

LR Carley, GGE Gielen, RA Rutenbar, WMC Sansen - DESIGN AUTOMATION CONFERENCE, 1996 -

[doi.ieeecomputersociety.org](#)

... any of the proposed standards. And, we do not cover analog and **mixed-signal simulation** strategies. These are much more mature than ...

Cited by 53 - [Web Search](#) - [BL Direct](#)

Hierarchy Based Statistical Fault Simulation of Mixed-Signal ICs - group of 5 »

G Devarayanadurg, P Goteti, M Soma - The 1996 IEEE International Test Conference, 1996 - [ieeexplore.ieee.org](#)

... **signal** circuits has been plagued by a num- ber of issues, the most important being:

1. **Mixed-signal** system **simulation** at the transistor level is CPU intensive. ...

Cited by 27 - [Web Search](#) - [BL Direct](#)

... **simulation-based** test program verification and fault **simulation** capabilities for **mixed-signal** ... - group of 3 »

P Caunegre, C Abraham - European Design and Test Conference, 1995. ED&TC 1995, ..., 1995 - [ieeexplore.ieee.org](#)

... Achieving **simulation-based** test program verification and fault **simulation** capabilities for **mixed-signal** systems Caunegre, P. Abraham, C. Siemens Automotive ...

Cited by 24 - [Web Search](#)

A tutorial introduction to research on analog and mixed-signal circuit testing - group of 4 »

LS Milor - ... on Circuits and Systems II Analog and Digital **Signal** ..., 1998 - [ieeexplore.ieee.org](#)

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MC Jeruchim, P Balaban, KS Shanmugan - 1992 - New York: Plenum

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mixed signal simulation

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[BOOK] **Mixed-Mode Simulation**

RA Saleh, AR Newton - 1990 - Kluwer Academic Publishers Norwell, MA, USA

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[BOOK] **Mixed-mode simulation and analog multilevel simulation**

RA Saleh, SJ Jou, AR Newton - 1994 - Kluwer Academic Publishers

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Addressing substrate coupling in mixed-mode ICs: simulation and power distribution synthesis - group of 2

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Advanced mixed-mode simulation techniques - group of 2 »

JE Kleckner - Ph. D. Thesis California Univ., Berkeley., 1984 - [adsabs.harvard.edu](#)

Title: Advanced mixed-mode simulation techniques Authors: Kleckner, J.

E. Affiliation: California Univ., Berkeley. Journal: Ph.D ...

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... , SJ Jou, AR Newton, MM Simulation, AM Simulation - Norwell, MA, 1994

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Rapid simulation of substrate coupling effects in mixed-mode IC's - group of 2 »

NK Verghese, DJ Allstot, S Masui - 1992 - [ieeexplore.ieee.org](#)

... 2. SUBSTRATE COUPLING SIMULATION Rapid Simulation of Substrate Coupling Effects

in Mixed-Mode ICs IEEE 1993 CUSTOM INTEGRATED CIRCUITS CONFERENCE 0-7803-0826-3 ...

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VHD e LDO: A new mixed mode simulation

H El Tahawy, D Rodriguez, S Garcia-Sabiro, JJ ... - Design Automation Conference, 1993, with EURO-VHDL'93. ..., 1993 - [ieeexplore.ieee.org](#)

... VHD e LDO: A new mixed mode simulation El Tahawy, H. Rodriguez, D. Garcia-Sabiro, S. Mayol, JJ ANACAD EES "Les Jardins de Maupertuis", Meylan; This paper ...

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Behavioral modeling phase-locked loops for mixed-mode simulation - group of 3 »

BAA Antao, FM El-Turky, RH Leonowich - Analog Integrated Circuits and Signal Processing, 1996 - Springer

... Behavioral Modeling Phase-locked Loops for Mixed-Mode Simulation ... Page 3. Behavioral

Modeling Phase-locked Loops for Mixed-Mode Simulation 47 ...

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Parasitic Characterization of Radio-Frequency (RF) Circuits Using Mixed-Mode Simulation - group of 3 »

J Jang, E Kan, L So, R Dutton, T Johansson, T ... - PROCEEDINGS OF THE IEEE CUSTOM INTEGRATED CIRCUITS ..., 1996 - [w1.875.telia.com](#)

Page 1. Parasitic Characterization of Radio-Frequency RF Circuits Using

Mixed-Mode Simulation Jaejune Jang, Edwin C. Kan, Lydia So, Robert W. Dutton ...

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The second generation motis mixed-mode simulator - group of 2 »

CF Chen, CY Lo, HN Nham, P Subramaniam - Proceedings of the 21st conference on Design automation, 1984 - [portal.acm.org](#)

... and a switch level approach for unit delay simulation. It provides logic and timing verification for general MOS circuits in a mixed-mode environment. ...

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- ☐ 1. **On the design of CMOS digital output drivers with controlled dl/dt**
Maloberti, F.; Torelli, G.;
[Circuits and Systems, 1991., IEEE International Symposium on](#)
11-14 June 1991 Page(s):2236 - 2239 vol.4
Digital Object Identifier 10.1109/ISCAS.1991.176824
[AbstractPlus](#) | [Full Text: PDF\(300 KB\)](#) IEEE CNF
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- ☐ 2. **A monolithic 10-bit A/D using I/SUP 2/L and LWT thin-film resistors**
Brokaw, A.P.;
[Solid-State Circuits, IEEE Journal of](#)
Volume 13, Issue 6, Dec 1978 Page(s):736 - 745
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- ☐ 3. **A 13-bit, 2.2-MS/s, 55-mW multibit cascade $\Sigma\Delta$ modulator in CMOS 0.7- μ m single-poly technology**
Medeiro, F.; Perez-Verdu, B.; Rodriguez-Vazquez, A.;
[Solid-State Circuits, IEEE Journal of](#)
Volume 34, Issue 6, June 1999 Page(s):748 - 760
Digital Object Identifier 10.1109/4.766809
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- ☐ 4. **A pipelined 13-bit 250-ks/s 5-V analog-to-digital converter**
Sutarja, S.; Gray, P.R.;
[Solid-State Circuits, IEEE Journal of](#)
Volume 23, Issue 6, Dec. 1988 Page(s):1316 - 1323
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- ☐ 5. **1.5 μ m CMOS gate arrays with analog/digital macros designed using common base arrays**
Kawada, S.; Hara, Y.; Isono, T.; Inuzuka, T.;
[Solid-State Circuits, IEEE Journal of](#)
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Marie, H.; Belin, P.;
[Solid-State Circuits, IEEE Journal of](#)
Volume 33, Issue 7, July 1998 Page(s):1009 - 1013



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Y Cheng, MC Jeng, Z Liu, J Huang, M Chan, K Chen, ... - IEEE Transactions on Electron Devices, 1997 - [ieeexplore.ieee.org](#)

... BSIM3v3 for **Analog/Digital** Circuit **Simulation** Yuhua Cheng, Member, IEEE, Min-Chie

Jeng, Member, IEEE, Zhihong Liu, Member, IEEE, Jianhui Huang, ...

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